



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,819	10/31/2003	James B. Skov	013628.00519 (02CXT0049C)	9523
77339 7590 08/11/2009 JACKSON WALKER (CONEXANT) 901 MAIN STREET, SUITE 6000 DALLAS, TX 75202				
EXAMINER				
JAMAL, ALEXANDER				
ART UNIT		PAPER NUMBER		
2614				
MAIL DATE		DELIVERY MODE		
08/11/2009		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/697,819

**Applicant(s)**

SKOV ET AL.

**Examiner**

ALEXANDER JAMAL

**Art Unit**

2614

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 April 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☐ Claim(s) \_\_\_\_\_ is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/55/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 1-7** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claim 1** recites an AC signal that is modulated, then a load is modulated when said AC signal is not modulated. The claim makes no sense ! If the AC signal is not modulated then the 'load modulating' step will never happen. Additionally it is not clear how exactly the 'load' is modulated. For the purpose of examination the examiner assumes the claimed system functions bi-directionally and can modulate/demodulate data in either direction based on the detection of incoming data.

Correction/Clarification is requested.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

Art Unit: 2614

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. **Claims 1-20** rejected under 35 U.S.C. 103(a) as being unpatentable over Rahamim (6351530), and further in view of Thomas (US 20040153543 A1).

As per **claims 1,8**, Rahamim discloses a system and method for sending digital clock signals across an isolation transformer combined with (modulating) a power signal (AC signal). The system uses a transmit and receive comparator to transmit/receive (extract) the bidirectional data across a separate transformer (comparators 400,402 in Fig. 5). However, Rahamim does not disclose a bidirectional data signaling protocol implemented where data signals are received bidirectionally across the same transformer as the AC power signal (modulating according to detected inbound data).

Thomas discloses a system where data is combined with (modulates) a power signal to form a bidirectional communications link (abstract). Thomas teaches that this allows the same set of lines to carry both power and data (para. 21). It would have been obvious to one of ordinary skill in the art at the time of this application to transfer both the modulated data and power over the same pair across the same transformer in order to eliminate the need for the data isolation transformer. The system can perform bidirectional data transmission (modulation/demodulation). The signals do not have to be present simultaneously, ie the outgoing modulation may be present when the incoming modulation is not present and vice-versa. The 'load modulation' must be 'sensed' in order to perform the disclosed bidirectional communication. It would have been obvious

to one of ordinary skill in the art at the time of this application to combine the data and power isolation interface in order to reduce part count.

As per **claim 2,9,15**, Thomas discloses that any known modulation means may be used by the system, but does not specify the specific type.

It would have been obvious to one skilled in the art that any well known modulating scheme (such as frequency, amplitude, or phase) could be used in order to perform the disclosed modulating step as a matter of design choice). All modulating schemes are derived from a clocked bitstream of data to be transmitted. Further the examiner contends that any well known logic devices such as exclusive OR and NOR gates could be used as a matter of design choice in order to set the clocking rate for the modulating/demodulating processes.

As per **claim 16**, the device inherently comprises a driver in order to drive the signals across the transformer.

As per **claim 17**, Rahamim discloses that the line impedance (impedance presented to the transformer) may be made programmable via received data (digital values) (Fig. 1, Col 4 lines 45-65). This inherently requires a switch-able impedance element across the transformer.

5. **Claims 3-7,10-14,18-20** rejected under 35 U.S.C. 103(a) as being unpatentable over Rahamim (6351530), and further in view of Thomas (US 20040153543 A1) and further in view of Sun (5056118).

As per **claims 3,10,18**, Rahamim and Thomas disclose power and data signals being transmitted across the same transformer, but do not disclose a clock signal embedded in the data signal.

Sun discloses a system to embed and recover clock signals from a data stream using a comparator (Fig. 1, Abstract). The clock signals are used to sample (recover) the data signals (abstract).

As per **claims 4,11,19**, the transitions are sensed with the comparator, and an independent clock is synchronized with a 'controllable oscillator' (Fig. 3, return to zero).

As per **claims 5,6**, any electrical signal present on the inputs to the transformer (such as an incoming clocked data signal or an outgoing analog signal) will vary the impedance presented to the transformer.

As per **claim 7,12**, Rahamim discloses that the line impedance (impedance presented to the transformer) may be made programmable via received data (digital values) (Fig. 1, Col 4 lines 45-65). This inherently requires a switch-able (analog gate) impedance element across the transformer.

As per **claims 13,14,20**, it is rejected as per claim 12 rejection. The system inherently comprises A/D and D/A converters for the purpose of sending and receiving the data/power.

***Response to Arguments***

1. Applicant's arguments have been fully considered but they are not persuasive.

As per applicant's argument that claims 1-7 are clear over the 112 rejection, the examiner disagrees. The examiner notes that applicant's response (remarks page 7) does nothing but repeat the claim elements and assert that they are clear. It is not clear what the phrase 'modulating according to inbound data the load presented to the second side of the transformer' means and it further is not clear what the phrase 'when the alternating current signal is not modulated' means. First of all it not clear what the AC signal would be modulated with (or 'not' modulated with), the incoming data, the outgoing data, both data? Additionally, the claim element of 'modulating a load presented to the second side of the transformer' is not clear. It is not clear if the element refers to **A**: sending modulated data across the transformer will change the impedance seen by the transformer (this is inherent for -any- transformer with a signal sent across it), or **B**: there is a circuit component varying an impedance component seen directly by the transformer side, with the varying done directly in proportion to modulated data sent on the AC the signal.

The examiner notes that examiner response to the 112 rejection was insufficient and the cited portion of the specification (page 10 lines 4-10) **does not** specify exactly

**how** or even in what manner the load is modulated. The examiner maintains the previous reading of the claim element, namely, that a modulated load is an inherent property to **any** transformer (including that of the prior art) with a signal modulated across it.

As per applicant's arguments that the cited prior art does not disclose the claim element of modulating a load presented to the secondary transformer side, the examiner contends that the claim element is not clear, the applicant has not cited -any- sections of the specification to clear up the claim element. The examiner maintains the reasonably broad reading of the claim element and contends that it is inherent to any transformer with modulated data transmitted across.

As per applicant's comments about the complexity of the Rahamim patent, the examiner notes the examiner's comments above which clearly disclose how the examiner is reading applicant's unclear claim element. The induced voltage across the transformer will change (modulate) the load seen by said transformer. The cited portions of the prior art clearly show a transformer with a data-modulated AC power signal sent across. The induced voltages will change the load impedance seen on the secondary side.

**Additionally**, the examiner contends that the prior art discloses modulators (which would be part of the 'load' seen by each side of the transformer). A modulator, when modulating one signal onto another will inherently modulate the load seen by the transformer because the modulated signal will create a transient value that was not there before. The capacitive and inductive portions of the 'load' will all react different to the new voltage transient added by the modulating signal, hence the load will be changed. This will happen in any system where a signal is modulated.



As per applicant's arguments that 'phase modulation' is not well known in the prior art, the examiner disagrees. The cited prior art discloses modulating an AC waveform with digital data for transmission across a transformer. Thomas states that any known modulation/demodulation scheme may be used. A phase modulation is a known type of modulation where a carrier signals phase is modulated according to data (a serial bitstream). All digital signal processing must be 'coincident with a clock' in order to be synchronized with the rest of the system. The obvious 'phase modulation' would inherently comprise a bitstream coincident with a clock in order to provide the modulating signal synchronized with the rest of the system. If the applicant maintains that 'coincident with a clock' is not inherent to any functional digital system, then the examiner notes that applicant's specification should be subject to a **112 first paragraph enablement** rejection as applicant's specification does not provide any timing diagrams or timing relationships between the various input/output signals. The examiner maintains that any digital processing stages require that all signals be coincident with a clock (or clocks) in order to be synchronized and function.

As per applicant's arguments concerning claim 15 and the claim element of sensing load modulations, the examiner refers to the above reading on how the load is modulated. The examiner contends that any demodulating stage across a transformer inherently senses the load modulations (via the measured voltage/current) of that transformer.

As per applicant's argument concerning claim 15 and the exclusive OR and NOR gates, the examiner notes that the disclosed digital demodulation stages require clocks in

order to synchronize all processing stages of the system. Claim 15 recites a signal modulator with exclusive OR and NOR gates. The examiner maintains that exclusive OR and NOR gates are well known types of logic gates that would be obvious to use to implement the desired timing for the disclosed demodulator. The examiner submits and notes US patent to Stevenson (6265948) (Fig. 3) which shows a modulator using the well known logic gates. The examiner additionally submits US patent to Chin-Chieh et al. (6977536) and Miyashita (6259723) Wang et al (6219380) which disclose the use of Xor and Xnor gates used to synchronize various digital circuits/processes. The examiner maintains that it would be obvious to implement XOR and XNOR gates as they are well known to be used for both signal modulating (which is disclosed by the prior art) and also in modulating timing signals for synchronization (which is inherently required as part of the disclosed modulating/demodulating steps). As per applicant's comment that the claim does not recite the XOR and XNOR gates being used to set the clocking rate for the modulating process, the examiner agrees, and notes that the claims only broadly and vaguely recite a signal modulator comprising an XNOR gate and an XOR. The examiner notes that a digital modulator inherently requires a clock, and accompanying clock deriving circuitry, and examiner notes that the XOR and XNOR gates as enabled by the specification, -are- used to set the clocking rate for the mod/demod process !

As per applicant's confusion with the word 'device' as used in the claim 16 rejection, the examiner notes that the 'device' is the device anticipated by Rahamim in view of the teachings of Thomas.

As per applicant's argument that signal drivers are not inherent to drive signals across the disclosed transformer, the examiner disagrees. Any signal must be driven with enough power in order to overcome the inherent impedance of the coupling connection. The prior art discloses a 'device' where power signals are modulated with bidirectional data. The modulated power signals require some sort of 'driver' in order to provide the signals with enough power to drive the transformer coil so as to induce the signal on the opposite transformer side. Any transmitted signal inherently requires a driver in order to 'drive' the signal across the transmission medium. The examiner further notes that Rahamim Fig. 5 discloses line drivers for each side of the isolation barrier (which may also be a transformer).

As per applicant's arguments that the claim 17 element of a transformer load modulator dependant upon received data is not disclosed in the prior art. The examiner notes the previously cited portion of Rahamim (Col 4 lines 55-67) discloses that the line side circuitry can be varied (such as changing the impedance) by data transmitted across the isolation barrier. This is the claimed 'transformer load modulator'.

As per applicant's comments in the claims 3,10,18,11,19,12, rejection that the processing step of Sun does not deal with demodulating data from an AC signal, the examiner notes that applicant is not considering the combination of references. Rahamim and Thomas disclose the demodulation of data from the AC power signal. Sun teaches an improved method of recovering modulated data (reception by the LIU) (Col 2 lines 35-60) with improved jitter protection. The examiner contends the demodulation disclosed by Rahamim and Thomas would obviously implement the clock recovery taught by Sun

in order to glean the advantage of improved jitter protection. Applicant says that Sun does not have anything to do with an AC signal modulated by digital data, and the examiner requests applicant read the entire background section of Sun to fully understand the scope of what Sun is talking about.

As per applicant's arguments about claim 4,12, every single digital processing stage in any device must be capable of sensing transitions (digital signaling). This includes the demodulator for the data modulated AC signal received across an isolation transformer disclosed by Rahamim/Thomas and the clock extracting recovery system disclosed by Sun. The modulating and demodulating circuitry will each have their own system clocks (required to function). Demodulating data inherently requires determining a clock to synchronize the recovered data to. The teachings of Sun disclose recovering a clock signal (by sensing transitions) and using said clock signal to recover the modulated data by synchronizing with a local independent clock (Col 2 lines 35-60).

As per applicant's arguments concerning claims 5,6,7 the examiner has not proposed any amendments for said claim. The examiner refers to the above comments regarding how the modulating load is read.

As per applicant's arguments (claim 13,14,20) that the A/D and D/A converters are not disclosed, the examiner contends that the modulator/demodulator stages taught by Rahamim and Thomas are the A/D D/A converters. **Additionally**, the examiner notes that Rahamim **further discloses additional A/D and D/A converters 188,190** to further convert the recovered data (Fig. 4b).

As per applicant's comment that using a D/A converter for sending power is absurd, the examiner requests applicant to review how a **switchmode regulator** works. That is but one example of a D/A used for power !

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Jamal whose telephone number is 571-272-7498, and whose email address is alexander.jamal@uspto.gov

The examiner can usually be reached on M-F 8AM-5PM.

Art Unit: 2614

If attempts to reach the examiner by telephone or email are unsuccessful, the examiner's supervisor, Curtis A Kuntz can be reached on 571-272-7499.

The fax phone numbers for the organization where this application or proceeding is assigned are **571-273-8300** for regular communications and **571-273-8300** for After Final communications.

/Alexander Jamal/

Primary Examiner, Art Unit 2614

Examiner Alexander Jamal

August 11, 2009